**Module: R5: RV-fpga**

**Section:** Installations **Task:** Tools

**Task 1.1**

**Tools**

* **Tools**
  + **RVfpga-ViDBo**

It uses a Nexys A7 board so that the program that simulates on the SOC can communicate with different peripherals.

* + **RVfpga-Trace**

It uses GTKWave for visualizing the internal signals of the SOC.

* + **RVfpga-Pipeline**

It uses SwerV EH1 core pipeline simulator for analyzing the execution of the different RISC-V instructions.

* + **RVfpga-Whisper**

Whisper is a RISCV instruction set simulator (ISS) developed for the verification of the SwerV micro-controller. It allows the user to run RISCV code without RISCV hardware. It comes integrated with PlatformIO.